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Eighth Semester B.Tech. Degree Examination, April 2014
(2008 Scheme)
08.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Define the terms :
   a) Clock rate
   b) CPI
   c) MIPS rate
   d) Throughput rate
2. State whether **each** of the following statements is **true** or **false** and justify your answer :
   a) The CPU computations and I/O operations cannot be overlapped in a multiprogrammed computer.
   b) As far as scalability is concerned, multicomputers with distributed memory are more scalable than shared-memory multiprocessors.
   c) Synchronization of all PEs in an SIMD computer is done by hardware rather than by software as is often done in most MIMD computer.
   d) In an MIMD computer, all processors must execute the same instruction at the same time synchronously.
3. What is the significance of Bernstein conditions in determining parallelism in a program ?

4. Draw a dependence graph to show all the dependences among the following statements.

   $S_1 : A = B + D$

   $S_2 : C = A \times 3$

   $S_3 : A = A + C$

   $S_4 : E = A/2$

5. Describe the possible hazards between read and write operations in an instruction pipeline.

6. Define pipeline throughput and efficiency.

7. Distinguish between typical RISC and CISC processor architectures.

8. Write a short note on Multiport memories in multiprocessor systems.

9. Distinguish between Write-through Caches and Write-Back Caches.

10. Differentiate between static and dynamic dataflow computers.

(10×4= 40 Marks)

PART – B

11. a) A workstation uses a 15-MHz processor with a claimed 10-MIPS rating to execute a given program mix. Assume a one-cycle delay for each memory access.

      i) what is the effective CPI of this computers ?

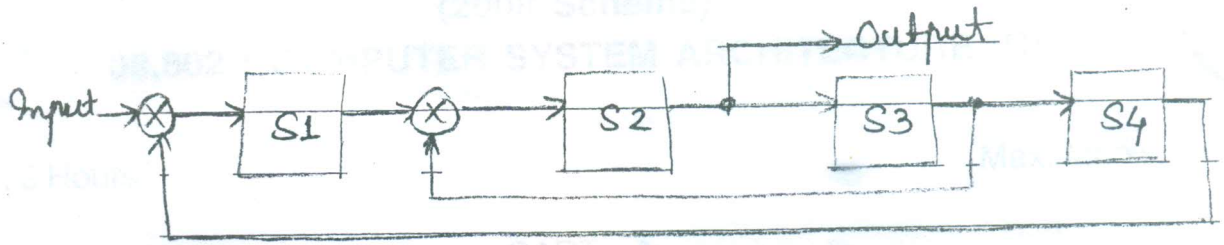
      ii) Suppose the processor is being upgraded with a 30 – MHz clock. However, the speed of the memory subsystem remains unchanged, and consequently two cycles are needed per memory access. If 30% of the instructions require one memory access and another 5% require two memory accesses per instruction, what is the performance of the upgraded processor with a compatible instruction set and equal instruction counts in the given program mix ? **12**

    b) Describe briefly about the operational model of SIMD computers with an example. **8**

OR

12 Explain the various dynamic interconnection networks used for contracting multiprocessors or multicomputers. Also compare their performances based on network characteristics. **20**

13. Consider the following pipelined processor with four stages. This pipeline has a total evaluation time of six clock cycles. All successor stages must be used after each clock cycle.



a) Specify the reservation table for this pipeline with six column and four rows.

b) List the set of forbidden latencies between task initiations.

c) Draw the state diagram which shows all possible latency cycles.

d) List all greedy cycles from the state diagram.

e) What is the value of the minimal average latency ?

f) What is the maximal throughput of this pipeline ? 20

OR

14 a) Explain how dynamic scheduling is achieved using Tomasulo's algorithm. 10

b) Explain the effect of branching and the various branch handling techniques used in instruction pipelining. 10

15. Explain the architecture of the Intel Paragon System with a neat schematic sketch. 20

OR

16. Explain the following Cache coherence protocol.
    a) Snoopy bus protocol
    b) Full map directory based protocol. 20